REMARKS

Claims 1-23 are pending. Claims 1-23 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over U.S. Patent No. 6,172,669 to Murphy et al. ("Murphy") in view of U.S. Patent No. 5,657,055 to Kansal et al. ("Kansal"). In view of the amendments and remarks herein, Applicant respectfully traverses the rejections and asks that they be withdrawn. Reconsideration and allowance are respectfully requested.

I. The Rejections under 35 U.S.C. 103(a)

Claim 1 - Hypothetical Combination Renders Murphy Unsuitable for Its Intended Purpose

Applicant respectfully submits that the hypothetical combination suggested in the Office Action would render Murphy unsuitable for its intended purpose, and therefore that the hypothetical combination would not be made by one having ordinary skill in the art. (Please see MPEP 2143.02).

In the Response to Arguments section, the Office Action alleges that the motivation to use an indicator in the line buffer originates in column 7, lines 25-30 of Murphy. However, the cited portion of Murphy concerns transfer of graphic data. In applying the cited portion of Murphy to the video line buffer, the interpretation of Murphy taken by the Office Action renders Murphy unsuitable for its intended purpose.

Murphy clearly teaches that the transfer of video data and graphic data occurs alternately, so that a lower bandwidth operation can be employed. (See the Abstract of Murphy). Murphy uses the following data transfer method in order to achieve its bandwidth advantage.

Murphy teaches that in a CRT monitor, displayed information is presented in the form of parallel scan lines. During the active portion of the scan, electron guns are scanning a line on the display. During the blanked part of the scan, the electron guns are reset from one side of the display to the other. (Please see column 6, lines 48-65 of Murphy).

Murphy teaches that during the active part of the scan, graphic data is transferred from the display buffer in a burst. (Please see column 7, lines 15-17 of Murphy). Note the scan line of video data that had previously been stored in the video line buffer is being displayed during the active part of the scan.

Video data for the next scan line is transferred to the video line buffer in a burst during the blanked part of the scan. (Please see column 7, lines 23-26 of Murphy). That is, an entire line of video data is transferred during the blank time. This line of video data is transferred during a time when video data is not being displayed.

If the suggested modification of Murphy were made, data would need to be transferred to the video line buffer during the active portion of the scan. That is, in order to transfer data to the video line buffer when it is half full, the transfer would need to be made halfway through the active portion of the scan. However, Murphy's system reserves the active portion of the scan for the transfer of graphic data.

Thus, the Office Action's suggested modification of Murphy renders Murphy unsuitable for its intended purpose. Rather than interleaving the transfer of graphic and video data and achieving the attendant reduced bandwidth, the Office Action suggests that video data be transferred during the time Murphy explicitly reserves for the transfer of graphic data. A person of ordinary skill in the art would not be motivated to make such a modification since it would contradict Murphy's express teaching.

Claim 1--The teachings of Kansal and Murphy do not provide a motivation for including an indicator in a video line buffer

Additionally, it is not obvious to modify Kansal to include the features of claim 1. Kansal is directed to systems and techniques for retrieving display data from a frame buffer into a CRT FIFO, where two MREQ priority levels are used. (Please see the Abstract of Kansal). When the level in the FIFO falls below the high level water mark, the MREQ generation circuit

generates a low priority MREQ signal. (Please see column 5, lines 14-18 of Kansal). When the level in the FIFO falls below the low level water mark, the MREQ generation circuit generates a high priority MREQ signal. (Please see column 5, lines 7-9 of Kansal).

Thus, Kansal is directed to systems and techniques for efficiently using the system memory bus by prioritizing the transfer of graphics data depending on the level of the graphics FIFO. When the level drops below the high level water mark, the graphics FIFO can receive more data, but the danger of FIFO underflow does not require that the graphics controller be given higher priority access to the system memory bus than other devices such as the CPU or I/O devices. However, once the level drops below the low level water mark, the graphics FIFO is in danger of underflowing, and is given priority over other devices.

Thus, the teachings of Kansal do not suggest using an indicator in a line buffer for video overlay data. The current inventors recognized that the features of claim 1 could enable the use of higher resolution display devices, by more efficiently integrating pixel processing with the display of video data. The indicator of claim 1 does not allow for more efficient use of the memory bus; in contrast, data may be transferred to the video line buffer from the video memory 205

more often using the indicator as claimed (e.g., data may be processed and transferred to the line buffer at the midpoint of reading the video data for the current scan line, as well as at the end of the scan line).

Stated differently, the problem addressed by Kansal, and its solution, do not apply to a video line buffer for video overlay data. The benefits achieved by Kansal would not accrue in a system including an indicator in a video line buffer. Further, there is no teaching or suggestion in either Kansal or Murphy of the shortcomings in the current methods for processing video line data noted by the current inventors, or that an indicator in the line buffer may be used to address these shortcomings.

For at least this additional reason, claim 1 is patentable over the combination of Kansal and Murphy.

Claims 2-23

Claims 2-23 either depend from claim 1, or include features similar to those discussed above with reference to claim 1, and so are patentable for at least the same reasons as outlined above.

Attorney's Docket No.:10559/170001/P8263/Intel Corporation

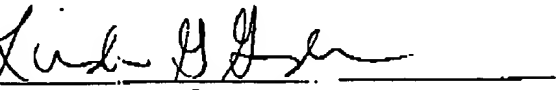
CONCLUSION

In view of the remarks herein, Claims 1-23 are in condition for allowance and a notice to that effect is respectfully solicited. The foregoing comments made with respect to the positions taken by the Examiner are not to be construed as acquiescence with other positions of the Examiner that have not been explicitly contested. Accordingly, Applicants' arguments for patentability of a claim should not be construed as implying that there are not other valid reasons for patentability of that claim or other claims.

If the Examiner has any questions regarding this response, the Examiner is invited to telephone the undersigned at (858) 678-5070. No fee is believed to be due at this time. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 5/10/04



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